Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

1. (original): A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

forming an insulating layer on the semiconductor substrate, including the gate pattern;

anisotropically etching the insulating layer to form sidewall spacers on both sidewalls of the gate pattern and to leave a portion of the insulating layer on the semiconductor substrate, wherein the gate pattern and the sidewall spacers constitute a gate structure;

injecting high concentration impurity ions of the second conductivity type into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure;

removing said portion of the insulating layer to expose an upper surface of the heavily doped region, wherein the lightly and heavily doped regions constitute a source/drain;

forming a transition metal layer over the semiconductor substrate, including the gate structure; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped regions.

2. (original): A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

forming sidewall spacers on both sidewalls of the gate pattern to form a gate structure consisting of the gate pattern and the spacers;

forming a buffering layer over the semiconductor substrate, including over the gate structure and the lightly doped regions;

with the buffering layer disposed over the lightly doped regions at both sides of the gate structure, injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure;

removing the buffering layer to expose an upper surface of the heavily doped regions and the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

once the buffering layer has been removed, forming a transition metal layer over the semiconductor substrate, including over the sidewall spacers and polysilicon gate of the exposed gate structure and the exposed heavily doped regions; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped regions;

wherein said buffering layer has a thickness sufficient to prevent the lightly doped regions from becoming damaged during said ion injection for forming said heavily doped regions.

3. (original): The method according to claim 2, wherein said transition metal layer is magnetic.

4. (original): The method according to claim 3, wherein said magnetic transition metal layer comprises at least one selected from a group consisting of cobalt, titanium, or nickel.

5. (original): The method according to claim 2, wherein said buffering layer comprises an insulator.

6. (original): The method according to claim 5, wherein said insulator comprises SiO.sub.2 or SiN.

7. (original): The method according to claim 2, wherein said thickness of said buffering layer is about 30Å..

8. (original): The method according to claim 2, wherein said transition metal layer is formed by physical vapor deposition or chemical vapor deposition using plasma.

9. (currently amended): A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

forming a buffering layer over the semiconductor substrate, including the gate pattern and the lightly doped regions;

forming sidewall spacers on a portion of the buffering layer at both sidewalls of the gate pattern to produce a gate structure;

injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

removing an exposed portion of the buffering layer to expose upper surfaces of the heavily doped regions and the polysilicon gate;

forming a transition metal layer over the semiconductor substrate, including the gate structure; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped region, wherein said annealing includes two annealing processes, and wherein one of said two annealing processes is a high temperature anneal executed at a temperature ~~of~~ which is at least 650°C ~~or more~~ and which is less than 750°C.

10 – 16. (cancelled)

17. (previously presented) The method according to claim 9, wherein said sidewall spacers are formed by an anisotropic etch.

18. (previously presented) The method according to claim 9, wherein said transition metal layer comprises cobalt, titanium, nickel, or a combination of two or more thereof.

19. (previously presented) The method according to claim 18, wherein said transition metal layer is formed by plasma vapor deposition (PVD) or chemical vapor deposition (CVD).

20. (previously presented) The method according to claim 19, wherein said PVD or CVD is carried out using plasma.

21. (previously presented) The method according to claim 9, wherein said low concentration impurity ions comprise Boron or Phosphorous.

22. (previously presented) The method according to claim 9, wherein said high concentration impurity ions comprise BF_2 or Arsenic.

23. (previously presented) The method according to claim 9, wherein the other of said two annealing processes is a low temperature anneal executed at a temperature of 400°C or more.

24. (previously presented) The method according to claim 23, wherein said low temperature anneal is executed between about 400°C and 500°C.

25. (previously presented) The method according to claim 23, wherein said low temperature anneal is executed prior to said high temperature anneal.

26. (previously presented) The method according to claim 9, wherein said buffering layer comprises an insulator.

27. (previously presented) The method according to claim 26, wherein said insulator comprises SiO2 or SiN.

28. (previously presented) The method according to claim 9, wherein the thickness of said buffering layer is about 30Å or more.